AF/2800

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPLICANT:	YOSHIDA, AKITO	DOCKET NO.:	W2K1077
SERIAL NO:	10/082,472	EXAMINER:	ZARNEKE
FILED:	02/22/2002	ART UNIT:	2827

TITLE: A STACKING STRUCTURE FOR SEMICONDUCTOR DEVICES USING A FOLDED OVER FLEXIBLE SUBSTRATE AND METHOD THEREFOR

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Weiss, Moy & Harris, P.C.
4204 N. Brown Avenue
Scottsdale, AZ 85251-3989

January 28, 2005

I hereby certify that on the 28th day of January, 2005, this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Jeffrey D. Moy

02/01/2005 HDEMESS1 00000075 10082472
01 FC:1402 500.00 OP

APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in triplicate in support of the Appeal in the above identified patent application. A check for the requisite fee of $500 is attached.

TABLE OF CONTENTS

REAL PARTY OF INTEREST

The present application is assigned to Amkor Technology, Inc., the real party of interest.

REALTED APPEALS AND INTERFERENCES

There are no related appeals and/or interferences pending.

STATUS OF CLAIMS

Claims 1-12 and 21-28 were rejected by the Examiner as noted in an Office Action dated May 11, 2004. A response was filed August 6, 2004 amending Claims 1-6, 10-12, and 21-28. In an Office Action dated October 19, 2004, the Examiner contends that the Amendment Letter dated August 6, 2004 is not fully responsive to the Office Action since amended claims 1, 11, and 21 are drawn to an invention that is independent or distinct from the invention originally claimed. The Examiner has withdrawn claims 1-30 from consideration as being directed to a non-elected invention.

STATUS OF AMENDMENTS

Applicant's understanding of the Examiner's Office Action dated October 19, 2004 is that the Amendment Letter dated August 6, 2004 has been entered but Claims 1-6, 10-12, and 21-28 have been withdrawn from consideration as allegedly being directed to a non-elected invention. However, it may be possible that the Examiner

never entered the Amendment Letter dated August 6, 2004. No Amendment was submitted in response to the Office Action dated October 19, 2004 or subsequent thereto.

SUMMARY OF THE INVENTION

The invention of Claims 1-12 and 21-28 encompasses a semiconductor stacking structure. The semiconductor stacking structure has a semiconductor device. A flexible substrate is coupled to a bottom surface of the semiconductor device. The flexible substrate is folded over on at least two sides to form flap portions. The flap portions are coupled to an upper surface of the first semiconductor device and cover only a portion of the upper surface of the semiconductor device.

ISSUES

Is the Examiner's withdrawal of pending Claims 1-12 and 21-28 as being directed to a non-elected invention properly made and well founded?

GROUPING OF CLAIMS

For purposes of this Appeal, Claims 1-12 and 21-28 stand or fall together as a group.

ARGUMENT

The claims as amended in the Amendment Letter dated August 6, 2004 are directed to the elected species made by Applicant in the Amendment Letter dated December 11, 2002 and the Examiner's withdrawal from consideration of pending Claims 1-12 and 21-28 as being directed to a non-elected invention is not properly made and should be reversed.

The Examiner has erroneously withdrawn Claims 1-12 and 21-28 from consideration for allegedly being directed to a non-elected invention.

The prosecution history for this case may be generalized as follows. In an Office Action dated October 18, 2002, the Examiner issued a restriction requirement directed towards then pending Claims 1-20. The Examiner stated that restriction to one of the following inventions was required: (I) Claims 1-12, drawn to a product, classified in Class 257, subclass 1+; and (II) Claims 13-20, drawn to a process, classified in Class 438, subclass 106+. In an Amendment Letter dated December 11, 2002, Applicant elected to prosecute the product Group (I) Claims 1-12 to prosecute and added additional Claims 21-28 all of which were drawn to a semiconductor stacking structure as shown and described in the patent application as originally filed.

Applicant has filed several Amendment Letters and an RCE in response to Office Actions sent by the Examiner. Each of the Amendment Letters further defined the elected Claims of the semiconductor stacking structure. In a first Office Action dated May 11, 2004 after the filing of the RCE, the Examiner rejected Claims 1-12 and 21-28 based on a new reference. In response to the May 11, 2004 Office Action, Applicant submitted an Amendment Letter dated August 8, 2004 amending Claims 1, 11, and 21 to further define the semiconductor stacking structure. The Examiner contends that the amended Claims 1, 11, and 21 are now independent or distinct from the originally presented Claims.

In Claim 1 as originally filed, Applicants claim:

> A semiconductor stacking structure comprising:
> a first semiconductor device; and
> a flexible substrate coupled to a bottom surface of the first semiconductor device wherein the flexible substrate is folded over on at least two sides to form flap portions which are coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device.

Applicant has amended Claims 1, 11, and 21 to claim the use of wirebonds for electrically coupling the semiconductor die to the metal layer. Claim 1 as now amended reads as follows:

> A semiconductor stacking structure comprising:
> a semiconductor die;
> a flexible tape substrate having at least one metal layer~~s~~ for electrical connections wherein the flexible tape substrate is coupled to a bottom surface of the semiconductor die;

wirebonds for electrically coupling the semiconductor die to the metal layer; and

an encapsulant covering the semiconductor die and the wirebonds;

wherein the flexible tape substrate further comprises a plurality of flap portions and each flap portion is folded along a side surface and an upper surface of the encapsulant;

wherein the flap portions do not over lap one another and cover only a portion of the upper surface of the encapsulant;

wherein the folded flap portions have an exposed metal layer.

Amended Claim 1, and similarly amended Claims 11 and 21, all relate to the semiconductor stacking structure elected and described in the specification and drawings as originally filed. The Claims have been refined to define the invention and to traverse the Examiner's rejection. The Examiner has cited no reason as to why or how the amendment directs Claims 1-12 and 21-28 to a non-elected invention. The Examiner issued a Restriction Requirement on product versus process Claims. Applicant elected to prosecute the product Claims and continues to prosecute the product Claims.

MPEP §803 states:

> Under the statute an application may properly be required to be restricted to one of two or more claimed inventions only if they are able to support separate patents and they are either independent (MPEP § 806.04 - § 806.04(i)) or distinct (MPEP § 806.05 - § 806.05(i)).
>
> Examiners must provide reasons and/or examples to support conclusions, but need not cite documents to support the restriction requirement in most cases.

The Examiner has failed to show how the amended Claims are "independent" or "distinct" as defined in MPEP § 802.01 from the elected product Claims. In order to be "independent", the Examiner must show "that there is no disclosed relationship between the two or more subjects." (MPEP § 802.01) The Examiner has failed to show any reason why the Claims as amended are unconnected in design, operation, or effect. The amended Claims withdrawn by the Examiner are directed to the same product elected and supported by the specification.

The Examiner has also failed to show how the amended Claims are "distinct" from the Claims as previously presented. In order to be "distinct", the Examiner must show that "two or more subjects as disclosed are related,... but are capable of separate manufacture, use, or sale as claimed, AND ARE PATENTABLE (novel and unobvious) OVER EACH OTHER (though they may each be unpatentable because of the prior art)." (MPEP § 802.01) (Emphasis included) The Examiner has failed to show the two requirements above to support his allegation that the amended Claims are "distinct" from the Claims as previously presented. Again, the amended Claims withdrawn by the Examiner are directed to the same product elected and supported by the specification. The amended Claims are a result of the prosecution history and for not claiming a distinct product.

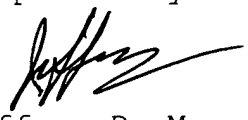
Therefore, the Examiner's statement dated October 19, 2004 that the Claims as amended in the Amendment Letter dated August 6, 2004 are directed to a non-elected invention should be reversed.

CONCLUSION

For the reasons stated above, the Claims as amended by Applicant are directed to the elected invention and that the Examiner's withdrawal of Claims 1-12 and 21-28 from consideration for allegedly being directed to a non-elected invention was improperly made and not well founded. Hence, Applicant respectfully urges the Board to reverse the Examiner's findings.

A check is attached in the amount of $500 for submission of a Brief in Support of Appeal. No additional fee or extension of time is believed to be required; however, in the event an additional fee or extension of time is required, please charge that fee or extension of time requested to our Deposit Account 23-0830.

Respectfully submitted,



Jeffrey D. Moy
Reg. No. 39,307
Attorney for Applicants

Weiss, Moy & Harris, P.C.
4204 N. Brown Ave.
Scottsdale, AZ 85251
(480) 994-8888 (Phone)
(480) 947-2663 (Fax)

JDM/msw

APPENDIX

1. A semiconductor stacking structure comprising:

a semiconductor die;

a flexible tape substrate having at least one metal layer~~s~~ for electrical connections wherein the flexible tape substrate is coupled to a bottom surface of the semiconductor die;

wirebonds for electrically coupling the semiconductor die to the metal layer; and

an encapsulant covering the semiconductor die and the wirebonds;

wherein the flexible tape substrate further comprises a plurality of flap portions and each flap portion is folded along a side surface and an upper surface of the encapsulant;

wherein the flap portions do not over lap one another and cover only a portion of the upper surface of the encapsulant;

wherein the folded flap portions have an exposed metal layer.

2. A semiconductor stacking structure in accordance with Claim 1 further comprising an adhesive layer which is placed on the flap portions of the flexible tape substrate and which couples the flap portions to the upper surface of the encapsulant.

3. A semiconductor stacking structure in accordance with Claim 1 further comprising an adhesive layer which is placed on the upper surface of the encapsulant and which couples the flap portions to the encapsulant.

4. A semiconductor stacking structure in accordance with Claim 1 further comprising a semiconductor device coupled to the flap portions of the flexible tape substrate.

5. A semiconductor stacking structure in accordance with Claim 4 wherein the semiconductor device is coupled to the flap portions of the flexible tape substrate after the flap portions are folded over and coupled to the encapsulant.

6. A semiconductor stacking structure in accordance with Claim 4 wherein the semiconductor device is coupled to the flap portions of the flexible tape substrate before the flap portions are folded over and coupled to the encapsulant.

7. A semiconductor stacking structure in accordance with Claim 1 wherein the semiconductor stacking structure is a LGA (Land Grid Array) device.

8. A semiconductor stacking structure in accordance with Claim 1 wherein the semiconductor stacking structure is a BGA (Ball Grid Array) device.

9. A semiconductor stacking structure in accordance with Claim 1 wherein the semiconductor stacking structure is a lead type of device.

10. A semiconductor stacking structure in accordance with Claim 1 wherein the flexible tape substrate is folded over on four sides to form flap portions which are coupled to the upper surface of the encapsulant and covers only a portion of the upper surface of the encapsulant.

11. A semiconductor stacking structure comprising:

a semiconductor die;

means for interconnection having at least one metal layers for electrical connections coupled to a bottom surface of the semiconductor die;

wirebonds for electrically coupling the semiconductor die to the metal layer; and

an encapsulant covering the semiconductor die and the wirebonds;

wherein the interconnection means further comprises a plurality of flap portions and each flap portion is folded along a side surface and an upper surface of the encapsulant;

wherein the flap portions do not over lap one another and cover only a portion of the upper surface of the encapsulant;

wherein the folded flap portions have an exposed metal layer.

12. A semiconductor stacking structure in accordance with Claim 11 further comprising an adhesive layer placed on the means for coupling the interconnection means to the upper surface of the encapsulant.

13 (Cancelled).

14 (Cancelled).

15 (Cancelled).

16 (Cancelled).

17 (Cancelled).

18 (Cancelled).

19 (Cancelled).

20 (Cancelled).

21. A semiconductor stacking structure comprising:

a semiconductor die;

means for interconnection having at least one metal layers for electrical connections coupled to a bottom surface of the semiconductor die;

wirebonds for electrically coupling the semiconductor die to the metal layer; and

an encapsulant covering the semiconductor die and the wirebonds;

wherein the interconnection means further comprises at least four flap portions and each flap portion is folded along a side surface and an upper surface of the encapsulant;

wherein the flap portions do not over lap one another and cover only a portion of the upper surface of the encapsulant;

wherein the folded flap portions have an exposed metal layer.

22. A semiconductor stacking structure in accordance with Claim 21 further comprising means placed on the flap portions of the flexible substrate for coupling the flap portions to the encapsulant.

23. A semiconductor stacking structure in accordance with Claim 21 further comprising means placed on the upper surface of the encapsulant for coupling the flap portions to the encapsulant.

24. A semiconductor stacking structure in accordance with Claim 21 further comprising a semiconductor device coupled to the flap portions of the coupling means.

25. A semiconductor stacking structure in accordance with Claim 24 wherein the semiconductor device is coupled to the flap portions of the coupling means after the flap portions are folded over and coupled to the encapsulant.

26. A semiconductor stacking structure in accordance with Claim 24 wherein the semiconductor device is coupled to the flap portions of the coupling means before the flap portions are folded over and coupled to the encapsulant.

27 (Cancelled).

28 (Cancelled).

29. A semiconductor stacking structure in accordance with Claim 1 further comprising an adhesive for coupling the semiconductor die to the flexible tape substrate.

30. A semiconductor stacking structure in accordance with Claim 11 further comprising an adhesive for coupling the semiconductor die to the means.